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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,786	03/12/2004	Yoshiaki Nakano	NAII122545	8315

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CHRISTENSEN, O'CONNOR, JOHNSON, KINDNESS, PLLC
1420 FIFTH AVENUE
SUITE 2800
SEATTLE, WA 98101-2347

EXAMINER	
CHIEM, DINH D	

ART UNIT	PAPER NUMBER
2883	

DATE MAILED: 01/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/799,786	NAKANO ET AL.
	Examiner	Art Unit
	Erin D. Chiem	2883

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/3/05*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 October 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____

Brian Healy
Primary Examiner

DETAILED ACTION

This office action is in response to the amendment filed on October 03, 2005. The objections to the drawings are withdrawn in view of the amendment. Currently, claims 1-15 are pending and claims 11-15 have been added in the amendment filed on May 23, 2005.

Claim Objection

Claim 1 and 10 are objected to because of the following informalities: the citation *–(a) remaining input port(s)—*is unclear. According to the MPEP §608.01 (m), the practice of employing parentheses in claims is generally for reference characters. However, as pointed out in the Examiner Note in form paragraph 7.29.02, if in the absence of the parentheses renders the claim indefinite, for example *–a remaining input ports--*, then a rejection under 35 USC 112 second paragraph is required. Since the lack of the parentheses only render the phrase improperly conjugated, therefore the examiner only object to the claim. Appropriate correction is required.

For the purpose of examination, the examiner will interpret the phrase in the singular form.

Claims 14 and 15 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. The preamble of claims 1, 14, and 15 reads *–the all-*

optical flip-flip--, one would presume that the set pulse and reset pulse are each light and are each an optical pulse.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ho et al. (US 6,788,838 B2 "Ho" hereinafter) in view of Chu et al. (US 6,522,462 "Chu" hereinafter).

Regarding claim 1, Ho teaches photon transistors, dubbed phosistor that function similarly as conventional transistors. The discussion of an optical flip-flop with a multi-mode interference configuration involves Figures 7, 7B, and 10. Figure 7 shows a general configuration of a phosistor, Figure 7B shows the configuration having the modification of a multi-mode interference configuration, and Fig. 10 shows the operation of an optical flip-flop with the multi-mode interference configuration. The phosistor comprises a waveguide (Fig. 10 element 1002 identified as Waveguide A), a plurality of input port (1006, 1010, 1014, 1016), an output port (1012 or 1014), and the input and output ports being connected to the multi-mode interference portion, with configuration being such that a set pulse from one or more input ports (1006) and a reset pulse from a remaining input port (1016), please refer to column 65, lines 34-45 for detail explanation.

Regarding claim 2, the limitation of oscillation based on the set pulse and the reset pulse generates different modes according to the set pulse and reset pulse, also mentioned in claim 1.

Since there is no other structurally limiting details regarding the set pulse and reset pulse, this is considered to be performance limitation, therefore the prima facie case of obviousness is established when the structural limitation is met.

Regarding claim 3, a plurality of output port is provided (1012, 1014).

Regarding claim 4, Ho teaches the input ports and the output ports are capable of allowing single mode light to pass by employing a mode-selective coupler (col. 65, line 9).

Regarding claim 5, Ho teaches the operation of the phosistor in the saturable absorption region is provided at the input ports and the output ports. Firstly, Figures 2-4 provides detail conceptual explanation of the electrons excitation states wherein the "active region" (M608) is operable in the transparent and absorption state. Furthermore, in one of the embodiment, Ho describes such medium as the "loss gate" wherein the absorbing or loss mode is in the input arm of the waveguide A. Although Ho does not explicitly state that the saturable absorption medium is specifically at the input and the output ports, but in view of applicant's disclosure the limitation is met. According to the applicant's teaching on page 4, first paragraph, "As is well known, absorption saturation occurs at the saturable absorption regions 34 when the power of inputted light exceeds a threshold value." Since there is no other structural detail that is patentably distinct from Ho's teaching of the phosistor comprising of semiconductor material, the examiner considers that the limitation is met.

Regarding claim 6, Ho broadly teaches that it is well-known in the art to employ reflective structures in the waveguides (col. 23, lines 3-4).

Regarding claim 7, wherein the input port doubles as the output port (1014) as taught in col. 64, line 67 to col. 65, line 2.

Regarding claim 8, mirror for reflecting inputted light is provided at the multi-mode interference is shown in Fig. 10, element (1030) at port (1014) since Ho teaches that 1014 doubles as input and output.

Regarding claims 11-13, these limitations are met through the structural limitations discussed above. Furthermore, it has been held that when the structure recited in the reference is substantially identical to that of the claims, claimed properties or functions are presumed to be inherent. *In re Ludtke, 441 F.2d 660, 169 USPQ 563.*

However, Ho only mentioned that the phosistor may be used as an optical diode and does not expressly teach that the phosistor is a semiconductor laser equipped with the limitations of claim 1 and 10. Nor does Ho explicitly teach using a circulator, even though a circulator is a species of a mode-selective coupler.

Chu teaches an all-optical logic device that integrates a semiconductor laser onto a single chip with the device by coupling a circulator (99, see Fig. 9) to the multi-mode interference portion.

Since Ho and Chu are both from the same field of endeavor, the purpose disclosed by Chu would have been recognized in the pertinent art of Ho.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to manufacture the optical flip-flop device integrally onto a single chip with the semiconductor laser. **The motivation** for integrating the laser with the flip-flop device is to reduce production cost and reduce the device size.

Response to Arguments

Applicant's arguments filed on May 23, 2005 have been fully considered but they are not persuasive. Applicant's argument regarding the cited reference character of the '180 reference does not teach a multi-mode interference portion but only teaches an active region is spurious since the examiner further cited Ho's further teaching that one skilled in the art would understand the active region (508) can be employed with a multi-mode interference device. However, in updating the prior art search, the examiner finds that the '810 reference is adequate, however, Ho's later patent, the '838 reference comprehensively teaches the main limitations of applicant's claims. Therefore this rejection is made NON-FINAL.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erin D. Chiem whose telephone number is (571) 272-3102. The examiner can normally be reached on Monday - Thursday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Frank G. Font can be reached on (571) 272-2415. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EDC

Erin D Chiem
Examiner
Art Unit 2883

Brian Healy
Primary Examiner